L Number	Hits	Search Text	DB	Time stamp
31	4	graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and control$3 and samples and pixels and (blocks or tiles) and fifo and ram and alu and @ad<20020228	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:16
32	4	graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and control$3 and samples and pixels and (blocks or tiles) and fifo and ram and alu and @ad<20020228	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:18
33	525	graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:34
34	30	graphics and (((level adj3 ("2" or two)) adj5 cache) same RAM) and ((level adj ("1" or one)) adj5 cache) same ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:37
35	23	(graphics and (((level adj3 ("2" or two)) adj5 cache) same RAM) and ((level adj ("1" or one)) adj5 cache) same ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) not sun not lavelle	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:43
36	0	20020129220.URPN.	USPAT	2004/03/02 18:40
37	0	((graphics and (((level adj3 ("2" or two)) adj5 cache) same RAM) and ((level adj ("1" or one)) adj5 cache) same ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) not sun not lavelle) and (memory adj3 request adj7 processor)	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:43
38	21	(graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:43
39	16	((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:44
40	12	(((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and "l1 cache"	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:44
41	0	(((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and "l3 cache"	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:44
42	12	(((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and (multiple adj5 cache)	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:45
43	8	(((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and (multiple adj5 cache) and ram and registers	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:45
44	7	((((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and (multiple adj5 cache) and ram and registers) and (modif$4 same cache)	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:46

45	7	((((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and (multiple adj5 cache) and ram and registers) and (modif$4 same cache) and graphics	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:46
46	8	((((graphics and ((level adj3 ("2" or two)) adj5 cache) and register and memory and @ad<20020228) and (memory adj3 request adj7 processor)) not sun not lavelle) and (multiple adj5 cache) and ram and registers) and (modif$4 or change or status same cache) and graphics	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:58
47	0		USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:59
48	100	("l3" adj3 cache) and (modif$4 or change or status same cache) and graphics and @ad<20020228	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:59
49	79	(("l3" adj3 cache) and (modif$4 or change or status same cache) and graphics and @ad<20020228) not sun not lavelle	USPAT; US-PGPUB; EPO; JPO	2004/03/02 18:59